Investigation of Drain Current Saturation in 4H-SiC MOSFETs

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Abstract. Electronic measurement coupled with device and material modeling of lateral long-channel 4H-SiC MOSFETs is used to investigate current saturation. Observed increases in drain current with increases in temperature are shown to result from a reduction in interface charge trapping. If trapping is ignored, the saturation current is predicted to decrease with increasing temperature as a result of interface phonon scattering.

Introduction

We report the investigation of current saturation in lateral 4H-SiC MOSFETs at high source-drain bias. In light of important applications for SiC in high temperature, high power electronics, it is necessary to understand the physical mechanisms impacting the saturation process. Our approach involves a close coordination between experimentation, device modeling, and the simulation of material properties. Results indicate that the saturation current \( I_{\text{DSAT}} \) in long-channel 4H-SiC MOSFETs depends on two important physical processes 1) the reduction of mobile charge due to interface trapping and 2) the scattering of mobile carriers with phonons. When trapping is significant, \( I_{\text{DSAT}} \) increases with increasing temperature since more induced interface charge is mobile \([1]\). If trapping is reduced, our results indicate a larger \( I_{\text{DSAT}} \) which decreases with increasing temperature due to phonon scattering. These results compare well with recent experiments in 4H-SiC MOSFETs with reduced trap concentrations \([2]\).

Experimentation

Electronic measurements have been taken on two 4H-SiC MOSFET devices (A, B), each processed distinctly. Both devices have a poly-silicon gate with 1X10\textsuperscript{19} cm\textsuperscript{-3} doping, a gate thickness of \( t_{\text{ox}}=60 \) nm, and a channel length (L), channel width (W) of 200 \( \mu \)m. Device A has a substrate acceptor doping of \( N_a=5x10^{15} \) cm\textsuperscript{-3} while device B is doped at \( N_a=1x10^{16} \) cm\textsuperscript{-3}. As seen in Fig 1, threshold voltage (\( V_{\text{th}} \)) measurements are temperature dependent. Furthermore, \( V_{\text{th}} \) is larger in device B indicating a net negative shift in fixed/trapped charge when compared to device A. Room temperature measurements in Fig.s 2-3 show that \( I_{\text{DSAT}} \) increases as the gate voltage (\( V_G \)) is increased. The rate of increase with \( V_G \) is however slow when compared to the familiar `square-law’ \( (I_{\text{DSAT}} \sim |V_G-V_{\text{th}}|^3) \), where \( V_{\text{th}} \) is the threshold voltage. On comparison, device A saturates at lower bias. As the temperature increases, an increase in the saturation current is measured in both devices.
Modeling and Simulation

**Charge Density** Device modeling is used to determine the temperature and voltage dependence of important charge densities in the 4H-SiC MOSFET [3]. These include mobile ($N_{\text{inv}}$), trapped ($N_t$), and fixed charge ($N_f$). Here $N_i$ and $N_f$ are effective densities, with all fixed and trapped charge constrained to lie exactly at the 4H-SiC/SiO$_2$ interface. Using measurements in Fig. 1, a determination of $N_f - N_i$ (at $V_g$) vs. semiconductor band bending ($\Psi_s$) at threshold can be made. This is accomplished by setting the threshold voltage minus the gate/semiconductor work function difference ($\varphi_{\text{ms}}$) equal to the total potential drop over the semiconductor (4H-SiC) and oxide:

$$V_{\text{th}}(T) - \varphi_{\text{ms}} = \Psi_s + e \int_{\text{ox}} \left[ \frac{2N_{f-t}}{\varepsilon_{\text{SiC}}} + \frac{N_f Z_d}{\varepsilon_{\text{SiC}}} \right].$$

The band bending and depletion width ($Z_d$) are found by self consistently solving for the mobile surface charge density using the threshold criteria $N_{\text{inv}} = N_a Z_{\text{AVG}}$, where $Z_{\text{AVG}}$ is the average channel depth.
Once $\Psi_s$ and $Z_d$ are found via self-consistent calculations, Eq. (1) can be solved for $N_{fv}$ as a function of surface band bending. Results are given in Fig. 4, where $N_{fv}$ decreases with increasing $\Psi_s$ due to an increase in trapped charge $N_t$. Since $N_t$ is independent of band bending, the curve can be extrapolated to low $\Psi_s$ to determine the fixed charge density (reported in the Fig. 4).

For gate voltages above threshold, the potential drop due to the mobile inversion charge must be taken into account by replacing $N_s Z_d$ with $N_{inv} Z_d$ in Eq. (1). As was the case at threshold, $\Psi_s, Z_d, N_{inv}$, and $Z_{av}$ are determined self-consistently. In this case, however, self-consistent calculations also satisfy Eq. (1) with $N_{fv}$ found directly from $\Psi_s$ using the threshold results in Fig. 4.

**Saturation Current** In order to model $I_{DSAT}$, a mobility model is needed. Considering phonon scattering, the conductivity mobility is modeled in terms of bulk (B) and surface (S) contributions:

$$\frac{1}{\mu_{mod el}} = \frac{1}{\mu_B} + \frac{1}{\mu_S}, \quad \mu_S = \frac{2eZ_{AVG}}{m^* v_{th} p}$$

where $e$, $m^*$, and $v_{th}$, are the charge, effective mass, and thermal velocity of an electron.

Furthermore, $p=0.11(T/300K)^{1.5}$ is the low-bias Fuchs parameter [3-5]. Here the bulk mobility ($\mu_B$), shown in Fig. 5, is determined using full-band Monte Carlo simulations considering acoustic, optical, and polar-optical phonon scattering. The surface mobility model ($\mu_S$) was found to agree with experiments at low source-drain bias and relatively large gate voltages in Fig. 6 [3].

The saturation current is modeled as a pinch-off mechanism according to

$$I_{DSAT} = e(N_{inv}) W \mu_{mod el} \left( \frac{V_G - V_{th}}{L} \right)$$

The average mobile charge density $\langle N_{inv} \rangle$ is found by averaging device modeling results for $N_{inv}$ from $V_G$ to $V_G-V_{th}$. As shown in Figs. 7-8, modeling and experiments agree well considering that the only adjustable parameter is the constant term in Fuchs parameter $p$. A value of 0.11 gives the best fit, this compares well with results in silicon (0.08) [5]. In device B, theory under predicts $I_{DSAT}$ near room temperature, further investigation is needed to resolve this issue.

The temperature behavior of $I_{DSAT}$ occurs since the ratio of mobile to total induced inversion charge $f$ (including trapped charge) in Fig. 9 increases drastically with temperature. In device A, $f$ increases with gate voltage indicating that increasingly more induced charge is mobile. However, $f$ is nearly independent of gate voltage in device B indicating that the rate of induced mobile and trapped charge is comparable in inversion. These differences in $f(V_G)$ are not yet understood.

If trapping is ignored in Fig. 10, $I_{DSAT}$ is predicted to decrease with increasing temperature due to phonon scattering. The temperature dependence of $I_{DSAT}$ is therefore a good indicator of trapping in 4H-SiC MOSFETs.
Summary

In this work we have presented an analysis of current saturation in lateral 4H-SiC MOSFETs. Threshold voltage measurements coupled with device modeling are used to determine important MOSFET charge densities as a function of experimental conditions. Furthermore, modeling results are used to develop a surface phonon mobility model sensitive to the channel depth. The bulk mobility contribution is found via Monte Carlo simulations. A theoretical model for the saturation current is developed using extracted charge densities and the theoretical mobility.

Experimental measurements of the $I_{DSAT}$ in two distinct devices are found to compare reasonably well with theory. Observed increases in $I_{DSAT}$ with temperature are found to be a direct result of increases in the amount of mobile induced charge. If charge trapping is reduced, $I_{DSAT}$ is predicted to decrease with temperature due to phonon scattering.

References

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